

Figure 15 shows the structure of the error correction device 100 of the present embodiment. According to the pipeline processing in error correction of the three ECC blocks, horizontal error correction in two ECC blocks and vertical error correction in the other ECC block are carried out at the same time. To realize the pipeline processing, in the error correction unit 100 of the present embodiment, the error corrector 7 has three mid-term result registers 81, 82, and 83, and the error corrector 6 outputs an error correcting position signal 24.

The behavior of the error correction device 100 of the present embodiment thus structured will be described as follows. While only one-time horizontal error correction is performed in Embodiments 1 through 5, the present embodiment performs error correction three times: in the horizontal direction, the vertical direction, and the horizontal direction in this order.

The pipeline processing in the three-time error correction is shown in Figure 16. At the first stage, horizontal error correction (the first-time error correction) is started only for the first ECC block. At the second stage, vertical error correction (the second-time error correction) is done for the first ECC block, and horizontal error correction (the first-time error correction) is started for the second ECC block. At the third stage, horizontal error correction (the third-time error correction) is done again for the first ECC block, the vertical error correction (the second-time error correction) is done for the second ECC block, and horizontal error correction (the first-time error correction) is started for the third ECC block.

In this manner, error correction for as many as three different ECC blocks is performed in parallel at the same stage, and at each stage the error correction is divided into plural steps. In the case of a DVD, the direction to read data for EDC calculation is the same as the syndrome calculation in the horizontal direction, and it is possible to perform EDC calculation in parallel with the syndrome calculation at the first-time and third-time error correction in the horizontal direction.

The flow of the process of the EDC calculation performed concurrently with the syndrome calculation at the third stage will be described with reference to Figures 15 and 16.

The first-time error correction for the third ECC block will be described as follows. The following steps (f1) through (f6) are basically the same as steps (d1) through (d6) in Embodiment 3, so that the procedure will not be illustrated.

Step (f1): in order to execute the first-time error correction for the third ECC block, the system control unit 1 outputs the DMA command 12 to the DMA control unit 2 so as to provide instructions to transfer data corresponding to a horizontal code word in the third ECC block from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

Step (f2): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

Step (f3): the bus control unit 3 puts the data bus 11 in commission, and outputs the buffer memory access signal 14 to the buffer memory 4 to read data therefrom. The bus control unit 3 then outputs the syndrome

data supply signal 15 and the error detector data supply signal 20 to the syndrome calculator 5 and the error detector 7, respectively, so as to supply the data read from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

Step (f-4): the syndrome calculator 5 calculates a syndrome 16 of the transferred horizontal code word, and outputs the syndrome 16 to the error corrector 6. If the code word contains an error-containing code or if the syndrome is not zero, the syndrome calculator 5 outputs the error-containing code detection signal 22 to the error detector 7 and to the system control unit 1. The syndrome calculator 5 also provides the system control unit 1 with the error-containing code word signal 23 indicating the code word from which an error has been detected in order to determine the code word to start the syndrome calculation and the valid range of an EDC in the third-time error correction.

The error detector 7 executes error detection for the transferred data in parallel with the syndrome calculator 5. Prior to the error detection, the mid-term results of the EDCs in the preceding code words stored in the first mid-term result register 81 are reloaded. If the syndrome is zero when the transfer of the code words is over, the mid-term results of the EDCs are stored in the first mid-term result register 81 again. When the syndrome is not zero, on the other hand, the mid-term results of the EDCs in the previous code words whose syndromes have been zero are maintained, without updating the contents of the first mid-term result register 81. In the first code word (the first line of the horizontal direction), the first mid-term result register 81 is initialized because it